IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulating layer and an SOI layer, comprising:

a MOS transistor provided in an element formation region of said SOI layer; and

a partial isolation region provided in said SOI layer and serving to isolate said element formation region, said partial isolation region including a partial insulating film provided in an upper layer portion of said SOI layer and a partial insulating film lower semiconductor region to be a part of said SOI layer present in a lower layer portion of said SOI layer,

said MOS transistor including:

source and drain regions of a first conductivity type selectively formed in said SOI layer, respectively;

a gate electrode having a gate electrode main part formed through a gate oxide film on a region of said SOI layer between said source and drain regions; and

a body region having a body region main part to be a region of a second conductivity type of said SOI layer between said source and drain regions and a body region potential setting portion electrically connected from said body region main part in said element formation region and capable of externally fixing an electric potential,

wherein said body region potential setting section includes a body region source/drain adjacent portion which is adjacent to ~~in a gate width direction adjacently to~~ said source and drain regions in a gate width direction and ~~extended in a gate length direction~~ which extends from said body region main part in a gate length direction,

said gate electrode further includes a gate extension region extended in said gate length direction from an end of said gate electrode main part and formed on a part of said body region source/drain adjacent portion, and serving to electrically block said body region

source/drain adjacent portion and said source and drain regions through said gate extension region, and

a thickness of said partial insulating film lower semiconductor region is thinner than a thickness of said source and drain regions.

Claim 2 (Canceled).

Claim 3 (Previously Presented): The semiconductor device according to claim 1, wherein

said body region source/drain adjacent portion includes a first body region source/drain adjacent portion extended in a first direction from said body region main part and a second body region source/drain adjacent portion extended in a second direction opposite to said first direction from said body region main part, and

said gate extension region includes a first gate extension region formed on a vicinity of said first body region source/drain adjacent portion and a second gate extension region extended on a vicinity of said second body region source/drain adjacent portion.

Claim 4 (Withdrawn): The semiconductor device according to claim 1, wherein

said body region source/drain adjacent portion includes one body region source/drain adjacent portion, and

said gate extension region includes one gate extension region formed on a vicinity of said body region source/drain adjacent portion.

Claim 5 (Withdrawn): The semiconductor device according to claim 1, wherein

said body region source/drain adjacent portion has a high concentration region having a higher impurity concentration of a second conductivity type than that in other regions over a region provided apart from said gate extension region by a predetermined distance.

Claim 6 (Withdrawn): The semiconductor device according to claim 1, wherein said gate extension region includes a gate extension region having an impurity concentration of the second conductivity type of 5×10^{18} cm^{-3} or less.

Claim 7 (Withdrawn): The semiconductor device according to claim 1, wherein said body region potential setting portion includes a semiconductor region for body fixation of the second conductivity type formed together with said source region.

Claim 8 (Original): The semiconductor device according to claim 1, wherein said partial isolation film lower semiconductor region has the second conductivity type and is formed in contact with said body region,

said semiconductor device further comprising:

an element formation region outside body region of a first conductivity type provided outside said element formation region of said SOI layer and being capable of externally fixing an electric potential, said element formation region outside body region being formed in contact with said partial insulating film lower semiconductor region.

Claim 9 (Original): The semiconductor device according to claim 1, wherein said source and drain regions have such depths as to reach said buried insulating layer.

Claim 10 (Original): The semiconductor device according to claim 1, wherein said source and drain regions have such depths that a depletion layer extended from said source and drain regions does not reach said buried insulating layer during a normal operation.

Claim 11 (Original): The semiconductor device according to claim 1, wherein said source and drain regions have such depths that said buried insulating layer is not reached and a depletion layer extended from said drain region reaches said buried insulating layer during a normal operation.

Claim 12 (Original): The semiconductor device according to claim 1, wherein said drain region has a greater depth than that of said source region and has such a depth that a depletion layer extended from said drain region reaches said buried insulating layer during a normal operation.

Claim 13 (Withdrawn): A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulating layer and an SOI layer, comprising:

first and second semiconductor regions of a predetermined conductivity type provided in an element formation region of said SOI layer; and

a partial insulating film provided in an upper layer portion of said element formation region and a partial insulating film lower semiconductor region of a predetermined conductivity type to be a part of said element formation region in a lower layer portion of said element formation region,

wherein said partial insulating film lower semiconductor region is electrically connected to said first and second semiconductor regions to constitute a resistive element.

Claim 14 (Withdrawn): The semiconductor device according to claim 13, further comprising:

a complete insulating film provided through said SOI layer for isolating said element formation region.

Claim 15 (Withdrawn): The semiconductor device according to claim 13, wherein said element formation region other than said partial insulating film and said first and second semiconductor regions is a part of a region where said resistive element is to be formed.

Claim 16 (Withdrawn): The semiconductor device according to claim 13, wherein said resistive element includes a load resistor of an SRAM memory cell.

Claim 17 (Withdrawn): A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulating layer and an SOI layer, comprising:

first and second element formation regions provided in said SOI layer;

a partial isolation region including a partial insulating film provided in an upper layer portion of said SOI layer and a semiconductor region to be a part of said SOI layer which is provided under said partial insulating film and serving to isolate said first and second element formation regions from each other; and

first and second MOS transistors formed in said first and second element formation regions, respectively,

wherein at least one of a structure of a body region, a structure of a gate electrode and presence/absence of body potential fixation in said first and second MOS transistors is varied to make transistor characteristics of said first and second MOS

transistors different from each other.

Claim 18 (Withdrawn): A semiconductor device having an SOI structure including a semiconductor substrate, a buried insulating layer and an SOI layer, comprising:

first and second element formation regions provided in said SOI layer;

a partial isolation region including a partial insulating film provided in an upper layer portion of said SOI layer and a semiconductor region to be a part of said SOI layer which is provided under said partial insulating film and serving to isolate said first element formation region from other regions;

a complete isolation region including a complete insulating film provided through said SOI layer and serving to isolate said second element formation region from other regions;

a first MOS transistor formed in said first element formation region; and a second MOS transistor formed in said second element formation region, wherein said first and second MOS transistors have different transistor characteristics.

Claim 19 (Withdrawn): A method of manufacturing a semiconductor device comprising the steps of:

(a) preparing an SOI substrate having an SOI structure including a semiconductor substrate, a buried insulating layer and an SOI layer;

(b) selectively forming a partial insulating film in an upper layer portion of said SOI layer, said partial insulating film constituting a partial isolation region for isolating first and

second element isolation regions in said SOI layer together with a semiconductor region to be a part of said SOI layer which is provided under said partial insulating film; and

(c) forming first and second MOS transistors in said first and second element formation regions,

wherein at said step (c), at least one of a structure of a body region, a structure of a gate electrode and presence/absence of body potential fixation in said first and second MOS transistors is varied to make transistor characteristics of said first and second MOS transistors different from each other.

Claim 20 (Withdrawn): A method of manufacturing a semiconductor device comprising the steps of:

(a) preparing an SOI substrate having an SOI structure including a semiconductor substrate, a buried insulating layer and an SOI layer;

(b) selectively forming a partial insulating film in an upper layer portion of said SOI layer, said partial insulating film constituting a partial isolation region for isolating said first element isolation region from other regions together with a semiconductor region to be a part of said SOI layer which is provided under said partial insulating film;

(c) selectively forming a complete insulating film through said SOI layer, said complete isolating film constituting a complete isolation region for isolating said second element formation region from other regions,

(d) forming a first MOS transistor in said first element formation region; and

(e) forming a second MOS transistor in said second element formation region,

wherein said steps (d) and (e) are performed such that said first and second MOS transistors have different transistor characteristics.

REMARKS

Favorable reconsideration of this application, in light of the present amendments and following discussion, is respectfully requested.

Claims 1 and 3-20 are pending; Claim 1 is amended; Claims 4-7 and 13-20 are withdrawn from consideration; and no claims are newly added or cancelled herewith. It is respectfully submitted that no new matter is added by this amendment.

In the outstanding Office Action, Claims 1 and 8-11 were rejected under 35 U.S.C. § 102(e) as anticipated by Matsumoto et al. (U.S. Pat. No. 6,455,894, hereafter Matsumoto); Claims 1 and 8-11 were rejected under 35 U.S.C. § 102(e) as anticipated by Kunikiyo (U.S. Pat. No. 6,545,318); and Claim 12 was rejected under 35 U.S.C. § 103(a) as unpatentable over Kunikiyo in view of Aoki et al. (JP 1-268063, hereafter Aoki).

Applicants acknowledge with appreciation the indication that Claims 3 and 12 contain allowable subject matter.[1] The present amendment is not believed to alter the allowable status of Claims 3 and 12.

With regard to the rejection of Claims 1 and 8-11 under 35 U.S.C. § 102(e) as anticipated by Matsumoto, that rejection is respectfully traversed.

The body region potential setting portion of Claim 1 includes the body region source/drain adjacent portion which is provided adjacent to the source and drain regions in a gate width direction in the element formation region. As a non-limiting example, the body region 12, illustrated in Figure 3 of the present application, is provided adjacent to the source and drain regions 51 and 61 in a gate width direction W.

In the outstanding Office Action at page 3, the body terminal region 3d, shown in Figures 1 and 3 of Matsumoto, is indicated as corresponding to the body region potential setting portion recited in Claim 1. However, as illustrated in Figure 3 of Matsumoto, the

[1] Claim 12 was indicated as allowed in the Advisory Action of July 25, 2003.

body terminal region 3d is isolated from the source and drain regions 6a and 6b by the partial insulating film 5b. More specifically, the body terminal region 3d of Matsumoto is isolated, without being adjacent to the source and drain regions 6a and 6b. By contrast, the body region potential setting portion of Claim 1 is provided adjacent to the source and drain regions in a gate width direction in the element formation region.

Accordingly, Applicants respectfully submit that independent Claim 1 patentably distinguishes over Matsumoto. Likewise, it is respectfully submitted that dependent Claims 8-11 patentably distinguish over Matsumoto for the reasons above-noted with regard to Claim 1. It is therefore respectfully requested that this rejection be withdrawn.

Regarding the rejection of Claims 1 and 8-11 under 35 U.S.C. § 102(e) as anticipated by Kunikiyo, that rejection is also traversed.

As earlier noted, Claim 1 (from which Claims 8-11 depend) recites that the body region potential setting portion includes the body region source/drain adjacent portion which is provided adjacent to the source and drain regions in a gate width direction in the element formation region.

At page 4 of the outstanding Office Action, the impurity region 111 illustrated in Figures 1-3 of Kunikiyo is indicated as corresponding to the body region potential setting portion of Claim 1. However, as is evident from the planar structure illustrated in Figure 2 of Kunikiyo, the impurity region 111 is isolated from the source and drain regions 7 and 8 by the isolation insulating film 4. More specifically, Kunikiyo describes that the impurity region 111 is isolated, without being adjacent to the source and drain regions 7 and 8.

By contrast, as earlier indicated, the body region potential setting portion recited in Claim 1 is provided adjacent to the source and drain regions in a gate width direction in the element formation region.

Therefore, as Kunikiyo fails to disclose or suggest the body region potential setting portion of Claim 1, it is respectfully submitted that independent Claim 1 patentably distinguishes over Kunikiyo. Similarly, Claims 8-11 are believed to patentably distinguish over Kunikiyo for at least the reasons above set forth with regard to Claim 1, and it is respectfully requested that this rejection be withdrawn.

Consequently, in view of the foregoing discussion and present amendments, it is respectfully submitted that this application is in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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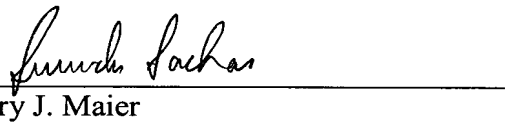

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